

Introduction

The 3GPP RACH Preamble Detector core provides an optimal solution for implementing RACH detection in a 3GPP uplink. The core includes all of the logic required for scramble-code generation, correlation, and preamble detection. The RACH Preamble Detector combines an optimal core and a flexible wrapper design, allowing custom implementation of detection algorithms and easy integration with a DSP or micro-processor.

Features

- Device families supported: Virtex™-4, Virtex-5, Spartan™-3A DSP
- Scalable solution for femto-cells up to macro-cells
- Algorithm Features
 - Compact, scalable correlation unit
 - Streamed correlation calculations, allowing minimal hardware use for femto and pico applications
 - Coherent and non-coherent result generation in parallel with correlation.
 - Sorted and filtered PDP results
- Design scales with following parameters to minimize resource utilization, based on:
 - Search window size
 - Coherent accumulation window size
 - Number of antenna
 - Oversample rate
 - Quantization
- Easy integration to microprocessor or DSP via OCP interfaces
- Pipelined read of RACH results for improved performance
- For use with the Xilinx CORE Generator™ software v9.2i and higher

System Overview

Figure 1 shows a typical use of the 3GPP RACH core. The core is designed to act as a co-processor attached to a microprocessor or DSP across a system bus. The open core protocol (OCP) interfaces allow easy adaptation to other bus protocols.

During operation, the RACH runs on every antenna on every slot. The processor can configure the RACH core over the OCP bus to determine the size of the cell being processed and the nature of the algorithm used to combine the RACH correlation data to form a decision. The antenna data stream can come directly from a radio interface, but could also be streamed via DMA across the system bus.

At the end of each slot, the RACH core produces a power delay profile (PDP) for each of the possible RACH preambles. These PDPs can then be read by the DSP. The core also produces an AICH recommendation based on the PDPs. This recommendation can be used by the processor, or it can interpret the PDPs to form its own decision. The PDPs are also required to initialize the searcher.

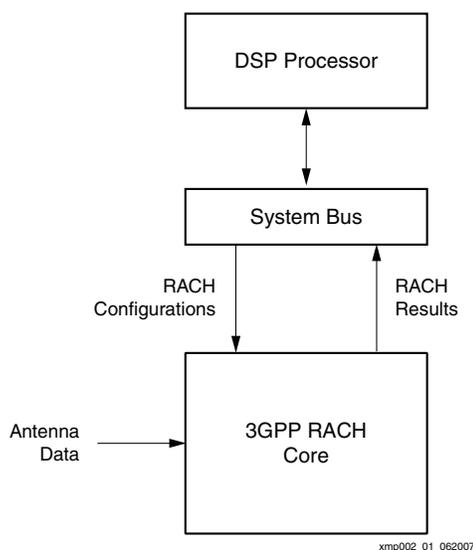


Figure 1: Typical Application

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Ordering Information

The 3GPP RACH core is provided under the [SignOnce IP Site License](#) and can be generated using the Xilinx CORE Generator software v9.2i or higher. The CORE Generator software is shipped with Xilinx ISE™ Foundation™ Series Development software.

Once purchased, the core may be downloaded from the Xilinx [IP Center](#) for use with the Xilinx CORE Generator software v9.2i and higher. The Xilinx CORE Generator software is bundled with the ISE Foundation software at no additional charge.

Contact your local Xilinx [sales representative](#) for pricing and availability of additional Xilinx LogiCORE™ modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

Revision History

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release